Pokhara University

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| Level: Bachelor | Semester – Fall | Year : 2011 |
| Programme: BE | | Full Marks: 100 |
| Course: Integrated Digital Electronics | | Pass Marks: 45 |
| Time : 3hrs. |

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| *Candidates are required to give their answers in their own words as far as practicable.* |
| *The figures in the margin indicate full marks.* |
| Attempt all the questions. |

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|  | 1. Draw and explain I/O characteristics of RTL inverter with its noise margins, transition width and logic swing. 2. Draw the IIL circuit with current injector and explain how it can be used as a decoder for 2 input variables. | 7  8 |
|  | 1. For the DTL NAND gate shown below, assume VCE (sat) = 0.2V, VBE(on) = VD(on) = 0.7V, VBE(sat) = 0.8V and ßF = 30. Calculate;    1. Fan out for output "High"    2. Fan out for output "Low"      1. Draw the high speed TTL circuit and explain how the following factors account for the high speed in it:    1. The input diodes    2. The darlington circuit    3. The active pull-down | 8  7 |
|  | 1. The OR output of the ECL gate is shown below to be fanned out to N similar gates. Find N at room temperature if the ∆1 noise margin is to be zero. Assume that the resistors of driving stage are 10% higher than typical and the resistors of driven stages are 10% lower than typical. The supply voltage is 5% higher and the transistor have current gains, hFE = 60. (The departures from the typical values are all in the direction to reduce the fan-out).The typical values are   RC2 = 300Ω, R4 =1500Ω, Re =1180Ω, and VEE =5.2 V.     1. Design CMOS NAND and NOR gate for 2 bit inputs. | 8  7 |
|  | 1. Explain read, write and refresh operations in a four-transistor MOS dynamic memory cell. 2. Discuss the operation of the three channel multiplexer circuit in detail. | 8  7 |
|  | 1. Compare the various bipolar logic families on the basis of switching speed and noise margin. 2. The rise time in NMOS is extremely long in comparison to the fall time whereas in case of CMOS both are almost equal. Why? 3. What is diode transmission gate? Discuss the operation with its limitation. | 4  3  8 |
|  | 1. What is entity and architecture design in VHDL? Explain with example. 2. Consider a simple digital circuit that warns car passengers when the door is open or the seatbelt is not used, whenever the car key is inserted in the ignition lock. Give the behavioural as well as the structural description of the circuit using VHDL. | 8  7 |
|  | Write short notes on **any two:**   1. High Threshold Logic 2. CCD (Charge Coupled Devices) 3. Active Pull UP | 2×5 |